

IN THE SPECIFICATION

Please rewrite the paragraph covering the entirety of page 17 as follows:

The diameter D1 of the spherical spacers 22 is theoretically given as

$$\begin{aligned} D1 &= (A+B+2C+D+E+F+G) - H-B-E-F-G \\ &= A+D+2C - H \text{ (micron)} \end{aligned} \quad (1)$$

where A is the thickness of the color filter 16 in micron, B is the thickness of the overcoat layer 11 in micron, C is the thickness of the orientation layer 9 in micron, D is the height of the column spacer 41 in micron, E is the thickness of the passivation layer 8 in micron, F is the thickness of the gate insulating layer 7 in micron, G is the thickness of the gate electrode 1 in micron and H is the thickness of the black matrix 17 in micron. The height D is measured from the boundary between the color filter 16 and the overcoat layer 11 to the boundary between the orientation layers 9. In actual products of the IPS liquid crystal display panel, the spherical spacers 22 are partially embedded in the overcoat layer 11 under the black matrix 17, and the spherical spacers 22 are designed in such a manner as to have the diameter D1' equal to or less than (D1 + 2) microns. Equation (1) is given on the assumption that there is a conductive layer patterned concurrently to the scanning lines 1 under the spherical spacers 22. If the gate insulating layer 7 is directly held in contact with the inner surface of the transparent insulating substrate 6a under the spherical spacers 22, the diameter D2 is given as

$$\begin{aligned} D2 &= (A+B+2C+D+E+F+G) - H-B-E-F \\ &= A+D+2C+G - H \text{ (micron)} \end{aligned} \quad (2)$$

Even so, the spherical spacers 22 are designed in such a manner as to have the diameter D1' equal to or less than (D1 + 2) microns.